FAIRCHILD SEMICONDUCTOR

March 2011

FDD3672_F085

N-Channel UltraFET Trench MOSFET

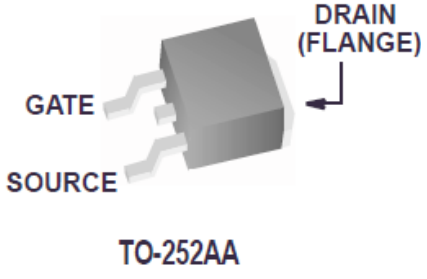
100V, 44A, 28mΩ

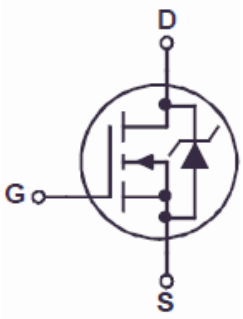
Features

- Typ $r_{DS(on)}$ = 24mΩ at V_{GS} = 10V, I_D = 44A
- Typ $Q_{g(10)}$ = 24nC at V_{GS} = 10V
- Low Miller Charge
- Low Q_{rr} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C < 30°C, V_{GS} = 10V)	44	A
	Pulsed	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	73	mJ
P_D	Power Dissipation	144	W
	Derate above 25°C	0.96	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	1.04	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient TO-263,1in² copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3672	FDD3672_F085	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
		T_J = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	3	4	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 44A, V_{GS}= 10V	-	0.024	0.028	Ω
		I_D = 21A, V_{GS}= 6V,	-	0.028	0.047	Ω
		I_D = 44A, V_{GS}= 10V, T_J = 175°C	-	0.063	0.074	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	1635	-	pF
C_{oss}	Output Capacitance		-	240	-	pF
C_{rss}	Reverse Transfer Capacitance		-	60	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V; V_{DD} = 50V, I_D = 44A, I_g = 1.0mA	-	24	36	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 to 2V; V_{DD} = 50V, I_D = 44A, I_g = 1.0mA	-	3	4.5	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50V, I_D = 44A, I_g = 1.0mA	-	8.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 50V, I_D = 44A, I_g = 1.0mA	-	5.3	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge	V_{DD} = 50V, I_D = 44A, I_g = 1.0mA	-	5.8	-	nC

Electrical Characteristics $T_J = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Switching Characteristics						
t_{on}	Turn-On Time	V_{DD} = 50V, I_D = 44A, V_{GS} = 10V, R_{GS} = 11Ω	-	-	78	ns
$t_{d(on)}$	Turn-On Delay Time		-	12	-	ns
t_r	Turn-On Rise Time		-	37	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	24	-	ns
t_f	Turn-Off Fall Time		-	44	-	ns
t_{off}	Turn-Off Time		-	-	70	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 44A	-	0.9	1.25	V
		I_{SD} = 21A	-	0.8	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 44A, dI_{SD}/dt = 100A/μs	-	44	57	ns
Q_{rr}	Reverse Recovery Charge		-	58	76	nC

Notes:

1: Starting $T_J = 25^oC$, L = 0.2mH, I_{AS} = 27A

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

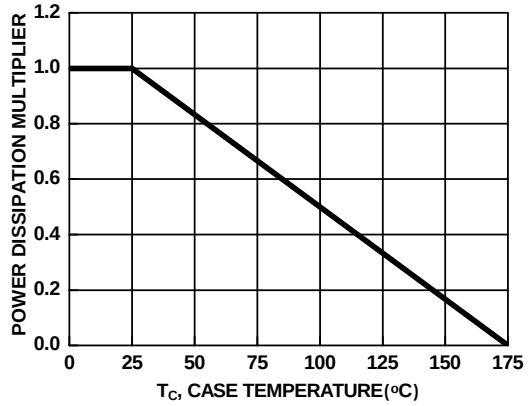


Figure 1. Normalized Power Dissipation vs Case Temperature

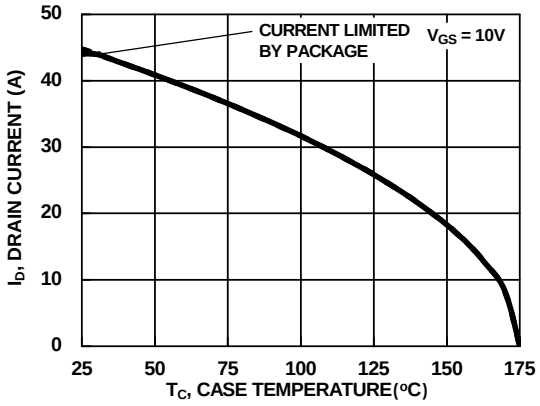


Figure 2. Maximum Continuous Drain Current vs Case Temperature

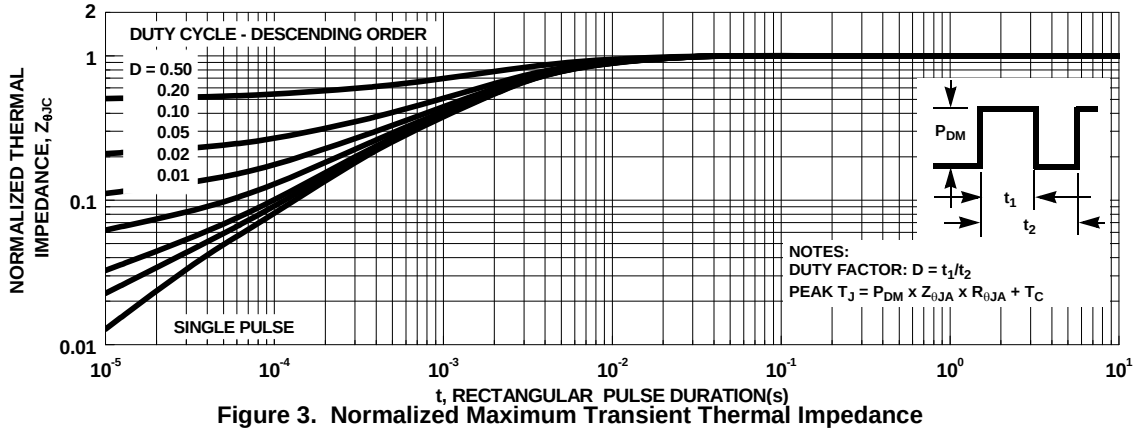


Figure 3. Normalized Maximum Transient Thermal Impedance

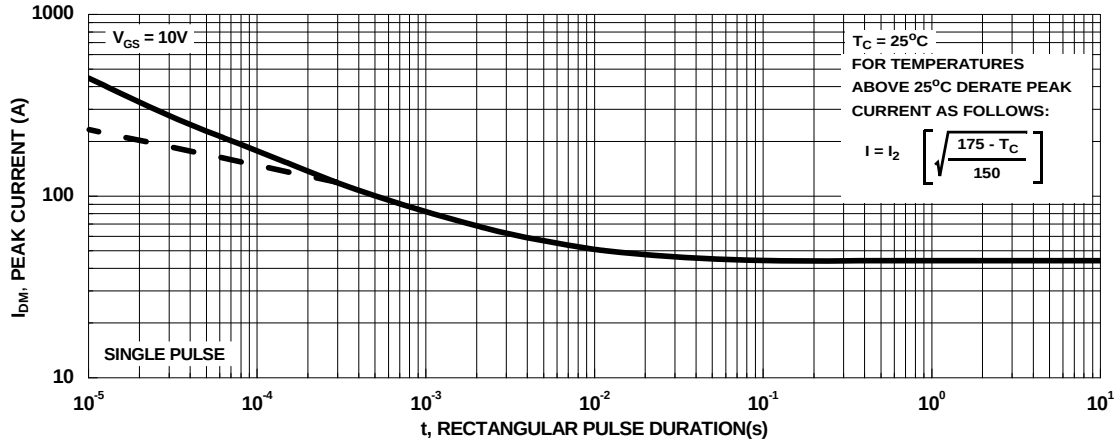


Figure 4. Peak Current Capability

Typical Characteristics

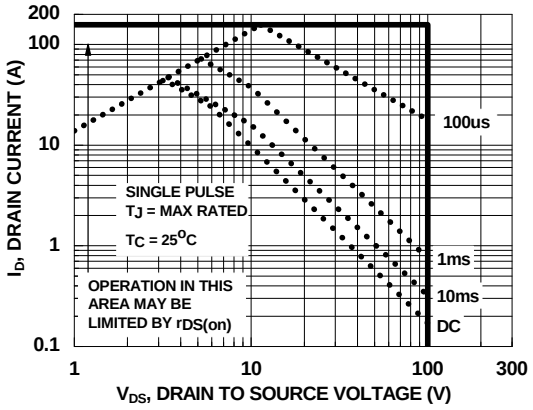
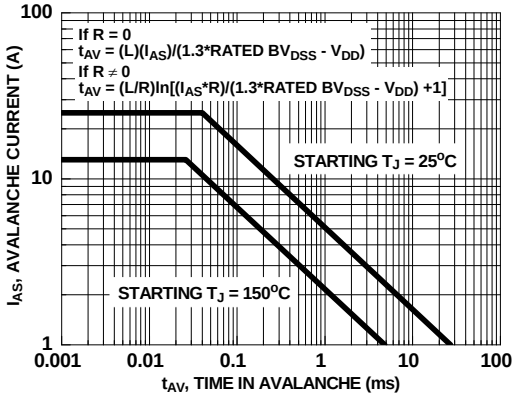


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

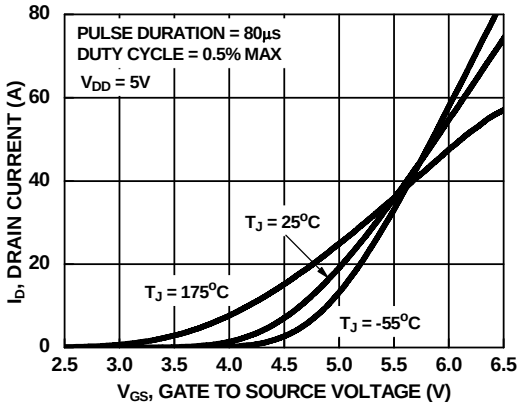


Figure 7. Transfer Characteristics

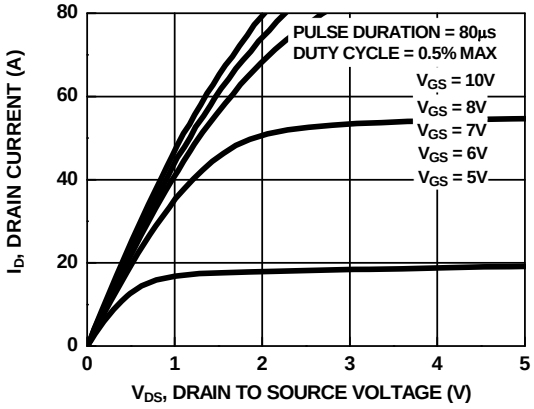


Figure 8. Saturation Characteristics

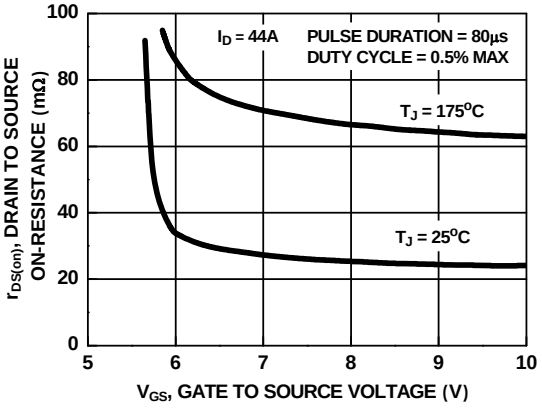


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

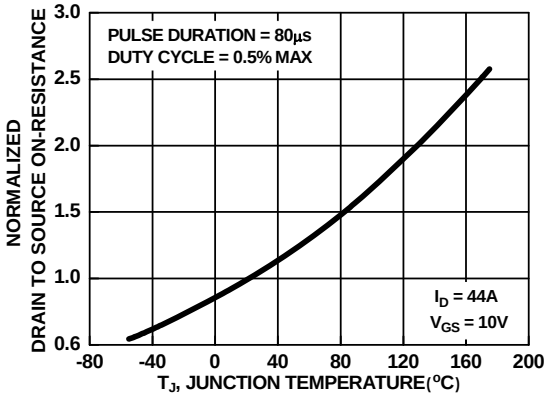


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

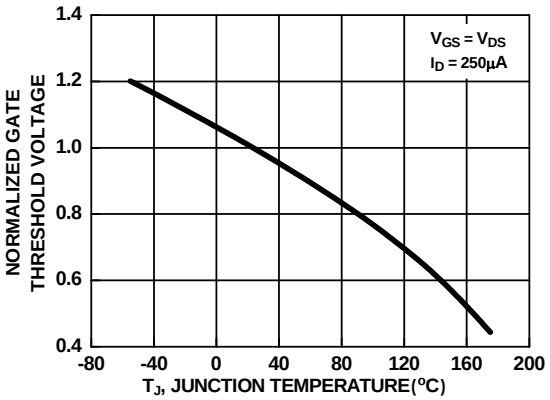


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

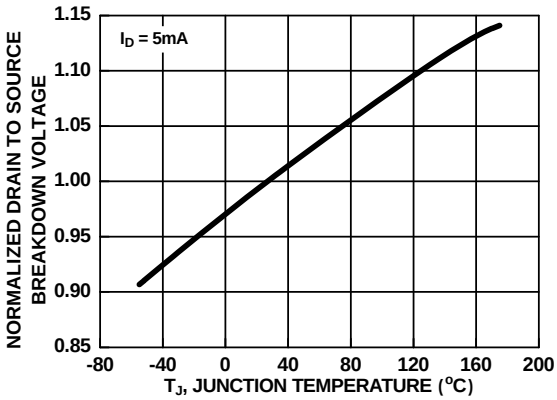


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

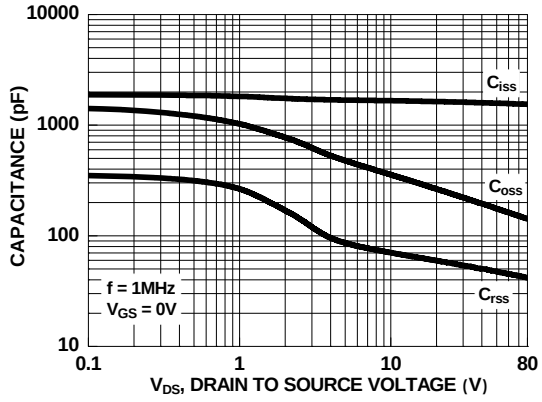


Figure 13. Capacitance vs Drain to Source Voltage

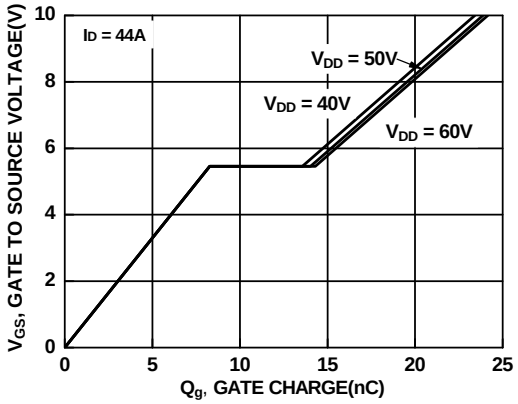


Figure 14. Gate Charge vs Gate to Source Voltage